WE CLAIM:

1   1.   An integrated circuit for selectively encrypting plaintext data received from a first device

2   to produce encrypted data to send to a second device, the integrated circuit comprising:

3   controllable encryption circuitry comprising:

4   a data input;

5   an enable input;

6   a data output;

7   a plaintext input for providing the plaintext data to the data input;

8   an encrypted text output for providing the encrypted data from the data output;

9   a first control input for receiving a first device authentication signal for

10   authenticating the first device; and

11   a first verification circuit, responsive to the first device authentication signal, for

12   producing a first verification signal for use in controlling the enable input of

13   the encryption circuitry to enable the encryption circuitry to provide the

14   encrypted data via the encrypted text output.

1   2.   The integrated circuit as recited in claim 1, further comprising:

2   a second control input for receiving a second device authentication signal

3   authenticating the second device;

4   a second verification circuit responsive to the second device authentication signal

5   for producing a second verification signal; and

6   a gating circuit responsive to the first and second verification signals for applying

7   an enable signal to the enable input to cause the controllable encryption

8   circuitry to provide the encrypted data via the encrypted text output.

1   3.   The integrated circuit as recited in claim 1, wherein:

2   the first device authentication signal comprises a device identifier; and

3   the first verification circuit verifies the first device by comparing the device

4   identifier to a corresponding expected device identifier.

1 4. The integrated circuit as recited in claim 3, wherein the expected device identifier is

2   hardwired into the integrated circuit.

1 5. The integrated circuit as recited in claim 3, wherein:

2   the second device is a non-volatile memory; and

3   the expected device identifier is stored on the non-volatile memory.

1 6. The integrated circuit as recited in claim 1, wherein:

2   the first device authentication signal comprises a message authentication code

3   generated over the plaintext data using a device key; and

4   the first verification circuit verifies the first device by verifying the message

5   authentication code using an internal key.

1 7. The integrated circuit as recited in claim 1, wherein:

2   the first device is a signal processing circuit; and

3   the second device is a non-volatile memory.

1   8.   A method of controlling encryption circuitry within an integrated circuit by selectively

2   encrypting plaintext data received from a first device to produce encrypted data to send to

3   a second device, the method comprising the steps of:

4   receiving the plaintext data from the first device;

5   receiving a first device authentication signal for authenticating the first device;

6   producing a first verification signal in response to the first device authentication

7   signal; and

8   enabling the encryption circuitry in response to the first verification signal to

9   provide the encrypted data to the second device.

1   9.   The method of controlling encryption circuitry as recited in claim 8, further comprising the

2   steps of:

3   receiving a second device authentication signal authenticating the second device;

4   producing a second verification signal in response to the second device

5   authentication signal; and

6   enabling the encryption circuitry in response to the first and second verification

7   signals to provide the encrypted data to the second device.

1   10.   The method of controlling encryption circuitry as recited in claim 8, wherein:

2   the first device authentication signal comprises a device identifier; and

3   the step of producing a first verification signal in response to the first device

4   authentication signal comprises the step of comparing the device identifier

5   to a corresponding expected device identifier.

1   11.   The method of controlling encryption circuitry as recited in claim 10, wherein the

2   expected device identifier is hardwired into an integrated circuit.

1   12.   The method of controlling encryption circuitry as recited in claim 10, wherein:

2   the second device is a non-volatile memory; and

3   the expected device identifier is stored on the non-volatile memory.

1 13. The method of controlling encryption circuitry as recited in claim 8, wherein:

2   the first device authentication signal comprises a message authentication code

3   generated over the plaintext data using a device key; and

4   the step of producing a first verification signal in response to the first device

5   authentication signal comprises the step of verifying the message

6   authentication code using an internal key.

1 14. The method of controlling encryption circuitry as recited in claim 8, wherein:

2   the first device is a signal processing circuit; and

3   the second device is a non-volatile memory.